We claim:

1. A semiconductor memory device, comprising:

a plurality of memory mats arranged in a direction of bit-line which including bit lines, word lines and memory cells coupled to said bit lines and said word lines;

a MOSFET included in each of said memory cells and having a capacitance having first and second electrodes, a gate coupled to a corresponding one of said word lines and source-and-drain paths one of which is coupled to a corresponding one of said bit lines and the other is coupled to said first electrode of said capacitance; and

a sense amplifier array provided in a region between said memory mats arranged in a direction of said bit line and having latch circuits having input/output nodes connected to a half number of bit line pairs provided to each of said memory mats,

wherein a failed bit line of said bit line pairs can be replaced, on a bit-line basis, with a redundant bit line and a corresponding redundant sense amplifier.

2. A semiconductor memory device according to claim 1, wherein said failed bit line is failed due to the presence of a failure on said memory cell itself.

3. A semiconductor memory device, comprising:

a plurality of memory mats arranged in a direction of bit-line which including bit lines, word lines and memory cells coupled to said bit lines and said word lines;

a MOSFET included in each of said memory cells and having a capacitance having first and second electrodes, a gate coupled to a corresponding one of said word lines and source-and-drain paths one of which is coupled to a corresponding one of said bit lines and the other is coupled to said first electrode of said capacitance; and

a amplifier circuit provided in a region between said memory mats arranged in a direction of said bit line and having unit-amplifier circuits connected to bit line pairs separately provided to two of said memory mats,

wherein the number of said unit-amplifier circuits being less than the number of said bit line pairs;and

wherein a failed bit line of said bit line pairs can be replaced, on a unit-amplifier basis, with a redundant bit line pair and a corresponding unit-amplifier circuit.

4. A semiconductor memory device according to

claim 3, wherein said bit line of said memory mat arranged in the bit-line direction is to be selected by a common Y-line select signal, and

said redundant bit-line pair and said unit-amplifier circuit are replaceable corresponding to each of said memory mats by the memory-mat select signal.

5. A semiconductor memory device according to claim 3, wherein said bit lines of said memory mat, as a center, that the failed bit line exists arranged on both sides with respect to the bit-line direction of said memory mat is to be replaced with said redundant bit line and said redundant unit-amplifier circuit.

6. A semiconductor memory device according to any of claims 3 to 5, wherein said failed bit line is failed due to the presence of a failure on said bit line itself.

7. A semiconductor memory device according to any of claims 3 to 6, wherein said bit lines to three memory mats of said memory mat having said failed bit line exist and said memory mats existing on both sides thereof are to be collectively replaced with corresponding redundant bit lines and redundant unit-amplifier circuits by a set of failure-address memory circuit for designating said failed bit line.

8. A semiconductor memory device according to claim 3, further including a plurality of first complementary input/output lines extended to said unit-amplifier circuits,

said unit-amplifier circuit including a pre-charge circuit to supply an intermediate voltage of operation voltage of said unit-amplifier circuit to said complementary bit line pair and

a pair of switch MOSFETS having a gate to receive the Y-select signal and provided between said bit line pair separately provided to two of said memory mats and said first complementary input/output line.

9. A semiconductor memory device according to any of claims 3 to 8, further including

a circuit for comparing memory means in an address of failure with an input address signal having fuse means to be selectively blown corresponding to an address of failure, a switch MOSFET provided between one end of said fuse means and a first voltage and supplied with a complementary address signal, and pre-charge means provided common to the other end of the fuse means to supply a pre-charge voltage having a second voltage; and

a circuit for forming an agreement/non-agreement

signal from the other end made common of said fuse means.

10. A semiconductor memory device, comprising:

a plurality of memory array regions arranged in a first direction;

a plurality of sense amplifier regions arranged alternate with said memory array regions;

each of said memory array regions having a plurality of bit lines extending in the first direction, a plurality of word lines extending in a second line orthogonal to the first line and a plurality of memory cells corresponding to said bit lines and said word lines;

each of said sense amplifier region having therein a first sense amplifier connected to a first bit line in one region of said memory array regions on adjacent both sides of each sense amplifier region and a second bit line in the other region thereof and a second sense amplifier connected to a first redundant bit line in said one region and to a second redundant bit line in the other region;

whereby, in the case that said first bit line in one memory array region is replaced with said first redundant bit line, said second bit line is to be replaced with said second redundant bit line.

11. A semiconductor memory device, comprising:

a plurality of memory array regions arranged in a first direction;

a plurality of sense amplifier regions arranged alternate with said memory array regions;

each of said memory array regions having a plurality of bit lines extending in the first direction, a plurality of word lines extending in a second line orthogonal to the first line and a plurality of memory cells corresponding to said bit lines and said word lines;

each of said sense amplifier region having therein a first sense amplifier connected to a bit line in one region of said memory array regions on adjacent both sides of each sense amplifier region and a bit line in the other region thereof and a second sense amplifier connected to a redundant bit line in said one region and to a redundant bit line in the other region;

whereby, in the case that a redundant bit line is selected in place of a predetermined bit line in one memory array region, said redundant bit line is selected in place of said predetermined bit line in another memory array region corresponding to said predetermined bit line in said one memory array

region.

12. A semiconductor memory device, comprising:

a plurality of memory array regions arranged in a first direction;

a plurality of sense amplifier regions arranged alternate with said memory array regions;

each of said memory array regions having a plurality of bit lines extending in the first direction, a plurality of word lines extending in a second line orthogonal to the first line and a plurality of memory cells corresponding to intersections between said bit lines and said word lines;

each of said sense amplifier region having therein a first sense amplifier connected to a first bit line in one region of said memory array regions on adjacent both sides of each sense amplifier region and a second bit line in the other region thereof and second sense amplifiers connected to first redundant bit lines in said one region and to second redundant bit lines in the other region;

whereby, effected in one memory array region are bit relief to replace said first bit line with said first redundant bit line

and bit relief, where in another memory array

region said redundant bit line is selected in place of a predetermined bit line, to select said redundant bit line in place of said predetermined bit line in said memory array regions on both sides of said other memory array region.

13. A semiconductor memory device, comprising:

a plurality of memory array regions arranged in a first direction;

a plurality of sense amplifier regions arranged alternate with said memory array regions;

each of said memory array regions having a plurality of bit line pairs extending in the first direction, a plurality of word lines extending in a second line orthogonal to the first line and a plurality of memory cells corresponding to ones of said bit line pairs and said word lines;

each of said sense amplifier region having therein a first sense amplifier connected to a first bit line in one region of said memory array regions on adjacent both sides of each sense amplifier region and a second bit line in the other region thereof and a second sense amplifier connected to a first redundant bit line in said one region and to a second redundant bit line in the other region;

whereby, effected in one memory array region can

be bit relief on a bit-line basis to replace said first bit line that failure exists on said memory cell with corresponding one of said first redundant bit lines

and bit relief on a bit-line-pair basis, when in one memory array region failure exists on said first bit line, both of said first and second bit lines can be replaced with said first and second redundant bit lines.

14. A Semiconductor memory device, including:

a first bit line;

a second bit line;

a first redundant bit line;

a second redundant bit line;

a plurality of first memory cells connected to said first bit line;

a plurality of second memory cells connected to said second bit line;

a plurality of first redundant memory cells connected to said first redundant bit line;

a plurality of second redundant memory cells connected to said second redundant bit line;

a first amplifier circuit connected to said first bit line and said second bit line to amplify a difference of potential between said first bit line

and said second bit line; and

a first redundant amplifier circuit connected to said first redundant bit line and said second redundant bit line to amplify a difference of potential between said first redundant bit line and said second redundant bit line,

wherein said first bit line is to be replaced with said first redundant bit line but said second bit line not to be replaced with said second redundant bit line.

15. A semiconductor memory device according to claim 14, wherein said first bit line and said first redundant bit line are included in a first memory array,

said second bit line and said second redundant bit line are included in a second memory array, and

said first amplifier circuit and said first redundant amplifier circuit being formed in a region between said first memory array and said second memory array.

16. A semiconductor memory device according to claim 15, wherein said second memory array further includes a third bit line,

said semiconductor memory device further including a third memory array including a fourth bit

line and a second amplifier circuit connected to said third bit line and said fourth bit line to amplify a potential difference between said third bit line and said fourth bit line; and

said second amplifier circuit being formed in a region between said second memory array and said third memory array.

17. A semiconductor memory device according to claim 14, wherein said first bit line, said second bit line, said first redundant bit line and said second redundant bit line are included in said first memory array,

said first bit line and said second bit line being arranged in parallel; and

said first redundant bit line and said second redundant bit line being arranged in parallel.

18. A semiconductor memory device according to claim 17, wherein said first memory array further including a third bit line and a fourth bit line,

said semiconductor memory device further including a second amplifier circuit connected to said third bit line and said fourth bit line to amplify a potential difference between said third bit line and said fourth bit line;

said first amplifier circuit and said first

redundant amplifier circuit being formed in a first region;

said second amplifier circuit being formed in a second region; and

said first memory array being formed in a region between said first region and said second region.

19. A semiconductor memory device according to claim 14, wherein said first bit line, said second bit line, said first redundant bit line and said second redundant bit line are included in a first memory array.

20. A Semiconductor memory device, including:

a first bit line;

a second bit line;

a first redundant bit line;

a second redundant bit line;

a plurality of first memory cells connected to said first bit line;

a plurality of second memory cells connected to said second bit line;

a plurality of first redundant memory cells connected to said first redundant bit line;

a plurality of second redundant memory cells connected to said second redundant bit line;

a first amplifier circuit connected to said

first bit line and said second bit line to amplify a difference of potential between said first bit line and said second bit line; and

a first redundant amplifier circuit connected to said first redundant bit line and said second redundant bit line to amplify a difference of potential between said first redundant bit line and said second redundant bit line,

wherein, in the case that said first bit line is failed and said second bit line is normal, said first bit line is replaced with said first redundant bit line and said second bit line is replaced with said second redundant bit line.

21. A semiconductor memory device according to claim 20, wherein said first bit line and said first redundant bit line are included in a first memory array,

said second bit line and said second redundant bit line are included in a second memory array, and

said first amplifier circuit and said first redundant amplifier circuit being formed in a region between said first memory array and said second memory array.

22. A semiconductor memory device according to claim 21, wherein said second memory array further

includes a third bit line,

said semiconductor memory device further including a third memory array including a fourth bit line and a second amplifier circuit connected to said third bit line and said fourth bit line to amplify a potential difference between said third bit line and said fourth bit line; and

said second amplifier circuit being formed in a region between said second memory array and said third memory array.

23. A semiconductor memory device according to claim 20, wherein said first bit line, said second bit line, said first redundant bit line and said second redundant bit line are included in said first memory array,

said first bit line and said second bit line being arranged in parallel and adjacent; and

said first redundant bit line and said second redundant bit line being arranged in parallel.

24. A semiconductor memory device according to claim 23, wherein said first memory array further including a third bit line and a fourth bit line,

said semiconductor memory device further including a second amplifier circuit connected to said third bit line and said fourth bit line to amplify a

potential difference between said third bit line and said fourth bit line;

said first amplifier circuit and said first redundant amplifier circuit being formed in a first region;

said second amplifier circuit being formed in a second region; and

said first memory array being formed in a region between said first region and said second region.

25. A semiconductor memory device according to claim 20, wherein said first bit line, said second bit line, said first redundant bit line and said second redundant bit line are included in a first memory array.

26. A Semiconductor memory device, including:

a first bit line;

a second bit line;

a first redundant bit line;

a second redundant bit line;

a plurality of first memory cells connected to said first bit line;

a plurality of second memory cells connected to said second bit line;

a plurality of first redundant memory cells connected to said first redundant bit line;

a plurality of second redundant memory cells connected to said second redundant bit line;

a first amplifier circuit connected to said first bit line and said second bit line to amplify a difference of potential between said first bit line and said second bit line; and

a first redundant amplifier circuit connected to said first redundant bit line and said second redundant bit line to amplify a difference of potential between said first redundant bit line and said second redundant bit line,

wherein, selectable are a case that said first bit line is replaced with said first redundant bit line but said second bit line is not replaced with said second redundant bit line and a case that said first bit line is replaced with said first redundant bit line and said second bit line is replaced with said second redundant bit line.

27. A semiconductor memory device according to claim 26, wherein said first bit line and said first redundant bit line are included in a first memory array,

said second bit line and said second redundant bit line are included in a second memory array, and

said first amplifier circuit and said first

redundant amplifier circuit being formed in a region between said first memory array and said second memory array.

28. A semiconductor memory device according to claim 27, wherein said second memory array further includes a third bit line,

said semiconductor memory device further including a third memory array including a fourth bit line and a second amplifier circuit connected to said third bit line and said fourth bit line to amplify a potential difference between said third bit line and said fourth bit line; and

said second amplifier circuit being formed in a region between said second memory array and said third memory array.

29. A semiconductor memory device, including:

a plurality of first normal bit lines;

a plurality of second normal bit lines;

a first redundant bit line;

a second redundant bit line;

a plurality of first normal memory cells connected to said plurality of first normal bit lines;

a plurality of second normal memory cells connected to said plurality of second normal bit lines;

a plurality of first redundant memory cells connected to said first redundant bit line;

a plurality of second redundant memory cells connected to said second redundant bit line;

a plurality of first amplifier circuits connected to said plurality of first bit lines and said plurality of second bit lines;

a second amplifier circuit connected to said first redundant bit line and said second redundant bit line to amplify a potential difference between said first redundant bit line and said second redundant bit line; and

an information hold circuit which holds information about replacement of a normal bit line into redundant bit line,

wherein each of said first amplifier circuits amplifies a potential difference between corresponding one of said first normal bit lines and corresponding one of said second normal bit lines;

said information hold circuit replacing one of said first normal bit lines into said first redundant bit line but not replacing one of said second normal bit lines corresponding to said one of said first normal bit lines into said second redundant bit line.

30. A semiconductor memory device according to

claim 29, wherein said information hold circuit can hold information to replace one of said second normal bit lines into said second redundant bit line but not to replace one of said first normal bit lines corresponding to said one of said second normal bit lines into said first redundant bit line.

31. A semiconductor memory device according to claim 29, wherein said information hold circuit can hold information that one of said first normal bit lines is to be replaced into said second redundant bit line and one of said second normal bit lines into said first redundant bit line.

32. A semiconductor memory device according to claim 29, wherein said information hold circuit can hold information that one of said first normal bit lines connected to one of said first amplifier circuits and one of said second normal bit lines are to be respectively replaced into said first redundant bit line and said second redundant line.

33. A semiconductor memory device according to claim 29, wherein said information hold circuit can hold information that one of said first normal bit lines connected to one of said first amplifier circuits is to be replaced into said first redundant bit line and one of said second normal bit lines

connected to another of said first amplifier circuits is to be replaced into said second redundant bit line.